Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A pulse output circuit comprising:

first to third input terminals;

an output terminal;

a first transistor including a first electrode electrically connected to the first input terminal;

a second transistor including a first electrode electrically connected to a power source;

a first amplitude compensation circuit;

a second amplitude compensation circuit; and

a capacitance means,

wherein:

channel regions of the first and second transistors have a same conductivity type;

each of a second electrode of the first transistor and a second electrode of the second transistor is electrically connected to the output terminal;

the capacitance means is provided between a gate electrode of the first transistor and the second electrode of the first transistor;

the gate electrode of the first transistor is electrically connected to an output terminal of the first amplitude compensation circuit;

a gate electrode of the second transistor is electrically connected to an output terminal of the second amplitude compensation circuit;

the second input terminal is electrically connected to each of a first input terminal of the first amplitude compensation circuit and a first input terminal of the second amplitude compensation circuit;

the third input terminal is electrically connected to a second input terminal of the second amplitude compensation circuit; and

the output terminal of the second amplitude compensation circuit is electrically connected to a second input terminal of the first amplitude compensation circuit.

2. (Original) A pulse output circuit comprising:

first to third input terminals;

an output terminal;

a first transistor including a first electrode electrically connected to the first input terminal;

a second transistor including a first electrode electrically connected to a power source;

a first second amplitude compensation circuit;

a second amplitude compensation circuit;

a capacitance means; and

a scanning direction switch circuit,

wherein:

channel regions of the first and second transistors have a same conductivity type;

each of a second electrode of the first transistor and a second electrode of the second transistor is electrically connected to the output terminal;

the capacitance means is provided between a gate electrode of the first transistor and the second electrode of the first transistor;

the gate electrode of the first transistor is electrically connected to an output terminal of the first amplitude compensation circuit;

a gate electrode of the second transistor is electrically connected to an output terminal of the second amplitude compensation circuit;

the second input terminal is electrically connected to a first input terminal of the first amplitude compensation circuit and to either a first input terminal of the second amplitude

compensation circuit or a second input terminal of the second amplitude compensation circuit via the scanning direction switch circuit;

the third input terminal is electrically connected to the input terminal of the first amplitude compensation circuit and to either the first input terminal of the second amplitude compensation circuit or the second input terminal of the second amplitude compensation circuit via the scanning direction switch circuit;

the output terminal of the second amplitude compensation circuit is electrically connected to a second input terminal of the first amplitude compensation circuit;

when the scanning direction switch circuit is in a first state, a signal inputted to the second input terminal is inputted to each of the first input terminal of the first amplitude compensation circuit and the first input terminal of the second amplitude compensation circuit, and a signal inputted to the third input terminal is inputted to the second input terminal of the second amplitude compensation circuit; and

when the scanning direction switch circuit is in a second state, a signal inputted to the second input terminal is inputted to the second input terminal of the second amplitude compensation circuit, and a signal inputted to the third input terminal is inputted to each of the first input terminal of the first amplitude compensation circuit and the first input terminal of the second amplitude compensation circuit.

3. (Original) A pulse output circuit comprising:

first to fourth input terminals;

an output terminal;

a first transistor including a first electrode electrically connected to the first input terminal;

a second transistor including a first electrode electrically connected to a first power source;

a third transistor including a first electrode electrically connected to a second power source;

a first amplitude compensation circuit;

a second amplitude compensation circuit; and

a capacitance means,

wherein:

channel regions of the first to third transistors have a same conductivity type;

each of a second electrode of the first transistor and a second electrode of the second transistor is electrically connected to the output terminal;

the capacitance means is provided between a gate electrode of the first transistor and the second electrode of the first transistor;

the gate electrode of the first transistor is electrically connected to an output terminal of the first amplitude compensation circuit;

a gate electrode of the second transistor is electrically connected to an output terminal of the second amplitude compensation circuit;

the second input terminal is electrically connected to each of a first input terminal of the first amplitude compensation circuit and a first input terminal of the second amplitude compensation circuit;

the third input terminal is electrically connected to a second input terminal of the second amplitude compensation circuit;

the output terminal of the second amplitude compensation circuit is electrically connected to a second input terminal of the first amplitude compensation circuit;

the fourth input terminal is electrically connected to a gate electrode of the third transistor; and

a second electrode of the third transistor is electrically connected to the gate electrode of the second transistor.

4. (Original) A pulse output circuit comprising:

first to third input terminals;

an output terminal;

a first transistor including a first electrode electrically connected to the first input terminal;

a second transistor including a first electrode electrically connected to a first power source;

a third transistor including a first electrode electrically connected to either a second power source or a gate electrode thereof;

a fourth transistor including a first electrode electrically connected to the first power source;

a fifth transistor including a first electrode electrically connected to the second power source;

a sixth transistor including a first electrode electrically connected to the first power source; and

a capacitance means,

wherein:

channel regions of the first to sixth transistors have a same conductivity type;

each of a second electrode of the first transistor and a second electrode of the second transistor is electrically connected to the output terminal;

the capacitance means is provided between a gate electrode of the first transistor and the second electrode of the first transistor;

each of a second electrode of the third transistor and a second electrode of the fourth transistor is electrically connected to the gate electrode of the first transistor;

each of a second electrode of the fifth transistor and a second electrode of the sixth transistor is electrically connected to a gate electrode of the second transistor and a gate electrode of the fourth transistor;

each of a gate electrode of the third transistor and a gate electrode of the sixth transistor is electrically connected to the second input terminal; and

a gate electrode of the fifth transistor is electrically connected to the third input terminal.

5. (Original) A pulse output circuit comprising:

first to third input terminals;

an output terminal;

a first transistor including a first electrode electrically connected to the first input terminal;

a second transistor including a first electrode electrically connected to a first power source;

a third transistor including a first electrode electrically connected to either a second power source or a gate electrode thereof;

a fourth transistor including a first electrode electrically connected to the first power source;

a fifth transistor including a first electrode electrically connected to the second power source;

a sixth transistor including a first electrode electrically connected to the first power source;

a capacitance means; and

a scanning direction switch circuit,

wherein:

channel regions of the first to sixth transistors have a same conductivity type;

each of a second electrode of the first transistor and a second electrode of the second transistor is electrically connected to the output terminal;

the capacitance means is provided between a gate electrode of the first transistor and the second electrode of the first transistor;

each of a second electrode of the third transistor and a second electrode of the fourth transistor is electrically connected to the gate electrode of the first transistor;

each of a second electrode of the fifth transistor and a second electrode of the sixth transistor is electrically connected to a gate electrode of the second transistor and to a gate electrode of the fourth transistor;

each of a gate electrode of the third transistor and a gate electrode of the sixth transistor is electrically connected to either the second input terminal or the third input terminal via the scanning direction switch circuit;

a gate electrode of the fifth transistor is electrically connected to either the second input terminal or the third input terminal via the scanning direction switch circuit;

when the scanning direction switch circuit is in a first state, a signal inputted to the second input terminal is inputted to each of the gate electrode of the third transistor and the gate electrode of the sixth transistor, and a signal inputted to the third input terminal is inputted to the gate electrode of the fifth transistor; and

when the scanning direction switch circuit is in a second state, a signal inputted to the second input terminal is inputted to the gate electrode of the fifth transistor, and a signal inputted to the third input terminal is inputted to each of the gate electrode of the third transistor and the gate electrode of the sixth transistor.

6. (Original) A pulse output circuit comprising:

first to fourth input terminals;

an output terminal;

a first transistor including a first electrode electrically connected to the first input terminal;

a second transistor including a first electrode electrically connected to a first power source;

a third transistor including a first electrode electrically connected to either a second power source or a gate electrode thereof;

a fourth transistor including a first electrode electrically connected to the first power source;

a fifth transistor including a first electrode electrically connected to the second power source;

a sixth transistor including a first electrode electrically connected to the first power source;

a seventh transistor including a first electrode electrically connected to the second power source; and

a capacitance means,

wherein:

channel regions of the first to seventh transistors have a same conductivity type;

each of a second electrode of the first transistor and a second electrode of the second transistor is electrically connected to the output terminal;

the capacitance means is provided between a gate electrode of the first transistor and the second electrode of the first transistor;

each of a second electrode of the third transistor and a second electrode of the fourth transistor is electrically connected to the gate electrode of the first transistor;

each of a second electrode of the fifth transistor, a second electrode of the sixth transistor and a second electrode of the seventh transistor is electrically connected to a gate electrode of the second transistor and to a gate electrode of the fourth transistor;

each of a gate electrode of the third transistor and a gate electrode of the sixth transistor is electrically connected to the second input terminal;

a gate electrode of the fifth transistor is electrically connected to the third input terminal; and

a gate electrode of the seventh transistor is electrically connected to the fourth input terminal.

7. (Currently Amended) A pulse output circuit according to claim 4 ~~or claim 5~~ further comprising:

a seventh transistor,

wherein a gate electrode of the seventh transistor is electrically connected to the second power source; and

the seventh transistor is provided between an output electrode of the third transistor and the gate electrode of the first transistor.

8. (Original) A pulse output circuit according to claim 6, further comprising:

an eighth transistor,

wherein a gate electrode of the eighth transistor is electrically connected to the second power source; and

the eighth transistor is provided between an output electrode of the third transistor and the gate electrode of the first transistor.

9. (Currently Amended) A pulse output circuit according to claim 4 ~~or claim 5~~, further comprising:

a seventh transistor including a first electrode connected to a gate electrode thereof; and

an eighth transistor including a first electrode electrically connected to the first power source,

wherein:

the seventh transistor is provided between an output electrode of the third transistor and the gate electrode of the first transistor;

a gate electrode of the eighth transistor is electrically connected to each of the gate electrode of the second transistor and the gate electrode of the fourth transistor; and

a second electrode of the eighth transistor is electrically connected to the gate electrode of the first transistor.

10. (Original) A pulse output circuit according to claim 6, comprising:

an eighth transistor including a first electrode connected to a gate electrode thereof; and

a ninth transistor including a first electrode electrically connected to the first power source,

wherein:

the eighth transistor is provided between an output electrode of the third transistor and the gate electrode of the first transistor;

a gate electrode of the ninth transistor is electrically connected to each of the gate electrode of the second transistor and the gate electrode of the fourth transistor; and

a second electrode of the ninth transistor is electrically connected to the gate electrode of the first transistor.

11. (Currently Amended) A pulse output circuit according to ~~any one of claims 1 to 10~~ claim 1,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

12. (Currently Amended) A pulse output circuit according to ~~any one of claims 1 to 10~~ claim 1,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

13. (Currently Amended) A shift register comprising a plurality of stages of a pulse output circuit according to ~~any one of claims 1 to 12~~ claim 1.

14. (Currently Amended) **[[A]]** An electronic equipment using a pulse output circuit according to ~~any one of claims 1 to 12 or a shift register according to claim 13~~ claim 1.

15. (New) A pulse output circuit according to claim 5 further comprising:

a seventh transistor,

wherein a gate electrode of the seventh transistor is electrically connected to the second power source; and

the seventh transistor is provided between an output electrode of the third transistor and the gate electrode of the first transistor.

16. (New) A pulse output circuit according to claim 5, further comprising:

a seventh transistor including a first electrode connected to a gate electrode thereof; and

an eighth transistor including a first electrode electrically connected to the first power source,

wherein:

the seventh transistor is provided between an output electrode of the third transistor and the gate electrode of the first transistor;

a gate electrode of the eighth transistor is electrically connected to each of the gate electrode of the second transistor and the gate electrode of the fourth transistor; and

a second electrode of the eighth transistor is electrically connected to the gate electrode of the first transistor.

17. (New) A pulse output circuit according to claim 2,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

18. (New) A pulse output circuit according to claim 3,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

19. (New) A pulse output circuit according to claim 4,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

20. (New) A pulse output circuit according to claim 5,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

21. (New) A pulse output circuit according to claim 6,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

22. (New) A pulse output circuit according to claim 7,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

23. (New) A pulse output circuit according to claim 8,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

24. (New) A pulse output circuit according to claim 9,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

25. (New) A pulse output circuit according to claim 10,

wherein a capacitance between the gate electrode and the second electrode of the first transistor is used as the capacitance means.

26. (New) A pulse output circuit according to claim 2,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

27. (New) A pulse output circuit according to claim 3,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

28. (New) A pulse output circuit according to claim 4,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

29. (New) A pulse output circuit according to claim 5,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

30. (New) A pulse output circuit according to claim 6,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

31. (New) A pulse output circuit according to claim 7,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

32. (New) A pulse output circuit according to claim 8,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

33. (New) A pulse output circuit according to claim 9,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

34. (New) A pulse output circuit according to claim 10,

wherein a capacitance formed of first and second films each comprising either one of an active layer material, a gate electrode material and a wiring material, and of an insulating film provided between the first and the second films is used as the capacitance means.

35. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 2.

36. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 3.

37. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 4.

38. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 5.

39. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 6.

40. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 7.

41. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 8.

42. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 9.

43. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 10.

44. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 11.

45. (New) A shift register comprising a plurality of stages of a pulse output circuit according to claim 12.

46. (New) An electronic equipment using a pulse output circuit according to claim 2.

47. (New) An electronic equipment using a pulse output circuit according to claim 3.

48. (New) An electronic equipment using a pulse output circuit according to claim 4.

49. (New) An electronic equipment using a pulse output circuit according to claim 5.

50. (New) An electronic equipment using a pulse output circuit according to claim 6.

51. (New) An electronic equipment using a pulse output circuit according to claim 7.

52. (New) An electronic equipment using a pulse output circuit according to claim 8.

53. (New) An electronic equipment using a pulse output circuit according to claim 9.

54. (New) An electronic equipment using a pulse output circuit according to claim 10.

55. (New) An electronic equipment using a pulse output circuit according to claim 11.

56. (New) An electronic equipment using a pulse output circuit according to claim 12.

57. (New) An electronic equipment using a shift register according to claim 13.